IN THE CLAIMS

1. (Currently amended) A voltage divider arrangement comprising a reference terminal (1), an input terminal (2) for receiving an input signal with respect to said reference terminal (1), an output terminal (3) for supplying an output signal with respect to said reference terminal (1), and a resistor arrangement (20) arranged on a substrate (50) and coupled between said input terminal (2) and said reference terminal (1), wherein a distributed compensation capacitance structure (10) for compensating the influence of a distributed parasitic capacitance is arranged between said resistor arrangement (20) and said substrate (50); wherein said distributed compensation capacitance structure (10) is separated from said resistor arrangement (20) and said substrate (50) by respective insulation layers (30, 40).

2. (Previously presented) A voltage divider arrangement according to claim 1, wherein said resistor arrangement (20) has a meandering shape.

3. (Previously presented) A voltage divider arrangement according to claim 2, wherein said resistor arrangement (20) is made of poly-silicon.

4. (Previously presented) A voltage divider arrangement according to claim 1, wherein said distributed compensation capacitance structure (10) comprises a conductor layer of a predetermined shape.

5. (Previously presented) A voltage divider arrangement according to claim 4, wherein said predetermined shape is a triangular shape.

6. (Previously presented) A voltage divider arrangement according to claim 4, wherein the width of said conductor layer in the horizontal direction is selected according to the following equation:

$$D_k = \frac{DR}{1 + \frac{k}{M+1-k}\frac{CCMP_{sq}}{CP_{sq}}}$$

wherein CP_{sq} denotes the parasitic capacitance per unit area of resistor, DR denotes the length of said resistor arrangement (20), k denotes an index of a segment of said transistor arrangement (20); M denotes the total number of segments of said transistor arrangement (20), $CCMP_{sq}$ denotes the distributed compensation capacitance per unit area of resistor and D_k denotes said width of said conductor layer.

7. (Canceled)